High Mobility Metal Oxide TFTs by Atomic Layer Deposition for AMOLED Display†

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Abstract

This study has successfully fabricated high-mobility oxide thin films using the ALD process, achieving a high mobility of 52 cm²/Vs in TFTs, along with a small threshold voltage (Vth) range on Gen 4.5 glass substrates. Through systematically optimizing structural and process parameters, the process window for ALD device fabrication has been thoroughly explored. Finally, the high-mobility oxide TFTs were employed to develop a 6-inch AMOLED panels featuring narrow bezels and high display brightness.

Author Keywords

Metal Oxide, TFT, High mobility, OLED

1. Introduction

With the advancement of display technology, oxide TFTs have gained widespread application in both LCD and AMOLED displays [1,2]. Compared to LTPS, oxide TFTs exhibit lower leakage current and better uniformity over large-area substrates, making them more suitable for large-sized AMOLED displays. In addition, relative to LTPO, oxide TFTs require fewer photo masks and have lower manufacturing costs. However, oxide TFTs still face several challenges in AMOLED display applications, such as limited carrier mobility, negative threshold voltage (Vth) shift in short-channel devices, and unsatisfactory stress stability. In particular, the relatively low mobility of oxide devices needs larger channel widths to achieve sufficient current drive, which can lead to larger panel bezels and reduced pixel density (PPI). In recent years, high-mobility oxides have become a major research focus in the display industry [3]. Common strategies for improving mobility include increasing the indium (In) content, reducing gallium (Ga) and zinc (Zn) concentrations, incorporating dopant elements, realizing crystalline oxides, designing multi-layer transport structures, and improving thin-film quality to minimize defects [4].

Recently, atomic layer deposition (ALD) has attracted significant interest for its capability to deposit high-quality thin films [5]. Compared to physical vapor deposition (PVD), ALD enables precise control the film composition by adjusting the cycle ratios of indium, gallium, and zinc precursors. The atomic-level controllable growth enables high dense films with lower defects. Additionally, by varying the elemental ratios at different deposition stages, multi-layer films can be fabricated. Based on these advantages, ALD oxide thin films are beneficial for achieving TFT devices with enhanced mobility and lower defect density, demonstrating significant application potential in high-mobility oxide AMOLED displays.

In this work, we fabricated a high mobility oxide TFT by ALD process. The device has a high mobility of 52 cm^2/Vs, and a small Vth range on Gen 4.5 glass. Furthermore, these highly reliable TFTs have been successfully integrated into a 6-inch flexible AMOLED panel.

2. Experimental Section

High-mobility oxide (HMO) thin films were deposited on G4.5 glass substrates by plasma-enhanced atomic layer deposition (PEALD). High purity (3-dimethylamimopropryl)-dimethyl indium (DADI), trimethylgallium (TMGa), and diethylzinc (DEZ) were employed as source materials. Argon was used as both carrier and purge gas, while O_2 served as the reactive gas. As illustrated in Figure 1, each deposition cycle include four sequential steps: precursor dosing, purge, reaction, and second purge. By implementing precise control over the In, Ga, and Zn content in each cycle, thin films with different elemental compositions were achieved.

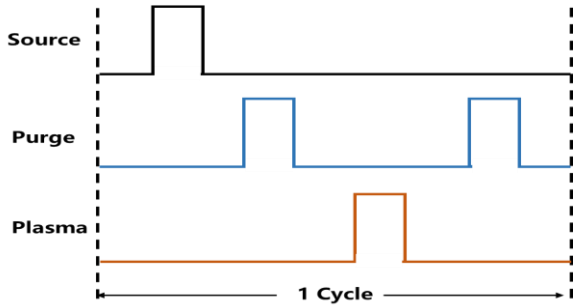


Figure 1. Oxide deposition cycles by PEALD

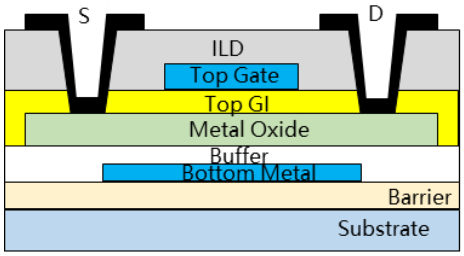


Figure 2. Structure of self-aligned TFT

The self-aligned metal oxide thin-film transistor (TFT) has been successfully engineered on a glass substrate in a Gen 4.5 AMOLED factory. The cross-sectional diagram of TFT's structure is shown in Figure 2, and this metal oxide TFT is fabricated as a top-gate structure with a bottom metal connected to source electrode. To optimize the film properties and fabrication process, this study systematically

investigated single-layer and multi-layer oxides, along with the optimized TFT process. Hall-effect measurements were employed to evaluate the Hall mobility and carrier concentration of different oxide layers. The High-resolution Transmission Electron Microscope (HTEM) was used to characterize the microscopic morphology of oxide layers, and energy dispersive spectroscopy (EDS) was used to analyze the crystalline nature and elemental information. The IDVG and BTS tests of different oxide devices were performed using a 4200 probe stage. The gate voltage range for All IDVG tests was set from -15 to 15 V, and the gate bias voltages of PBTS/NBTS tests were 30 V and -30 V, respectively, at temperature of 60 °C for 1 hour.

3. Results and Discussion

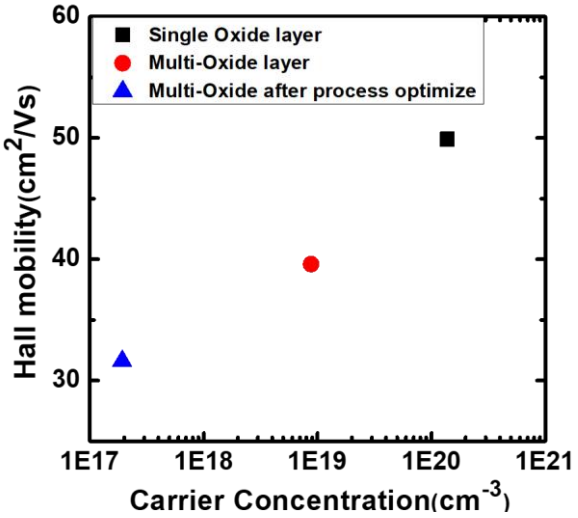


Figure 3. Hall Mobility of single layer, multi-layer and multi-layer after optimized TFT process.

The ALD process is typically performed at high temperatures, which can increase the carrier concentration in the oxide thin films. This can result in Vth negative shifts during oxide TFT fabrication. Therefore, it is critical to choose appropriate structures and optimize processes to reduce carrier concentration in ALD oxide device preparation. As shown in Figure 3, the Hall mobility results of ALD oxides include single-layer, multi-layer, and multi-layer after optimized TFT process. The multi-layer structure follows a low-mobility/high-mobility/low-mobility (L/H/L) stack layer. The single-layer oxide has a high mobility of 52cm²/Vs with a carrier concentration reaching the 1E21 level, which tends to cause negative threshold voltage shifts in devices. By adopting the L/H/L stacked structure, both carrier concentration and Hall mobility decrease, potentially due to carrier trapping by the low-mobility layer. After optimized TFT process, the carrier concentration in the multi-layer oxide is further suppressed, providing a larger process window for device fabrication.

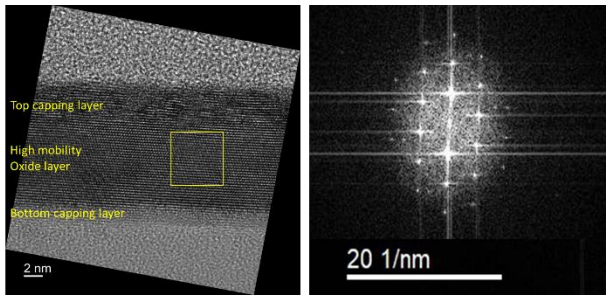


Figure 4. The HTEM image of multi-layer oxide, (a) sectional view, (b) EDS image of high mobility layer.

Figure 4 presents the HTEM images of multi-layer oxides. The multi-layer semiconductor structure comprises a bottom capping layer, a high-mobility layer, and a top capping layer. The bottom capping layer, positioned at the bottom of the stack and adjacent to the underlying SiOx layer, serves to suppress the diffusion of carriers and defects from the substrate into the channel. By selecting an oxide material with lattice parameters closely matching the high-mobility layer, it promotes epitaxial growth of the upper high-mobility layer and reduces its defect density. The high-mobility layer is composed of a crystalline oxide with high indium (In) content, exhibiting an ordered atomic arrangement and minimal film defects, which enables superior carrier mobility. The top capping layer, located at the top interface with the overlying SiOx layer, is a low-mobility oxide that effectively blocks carriers and defects migration from the top into the channel, preventing negative threshold voltage shifts. This multi-layer oxide configuration achieves low carrier concentration, high mobility, and robust defect blocking capability, making it ideal for realizing stability and convergence of Vth in ALD high-mobility devices.

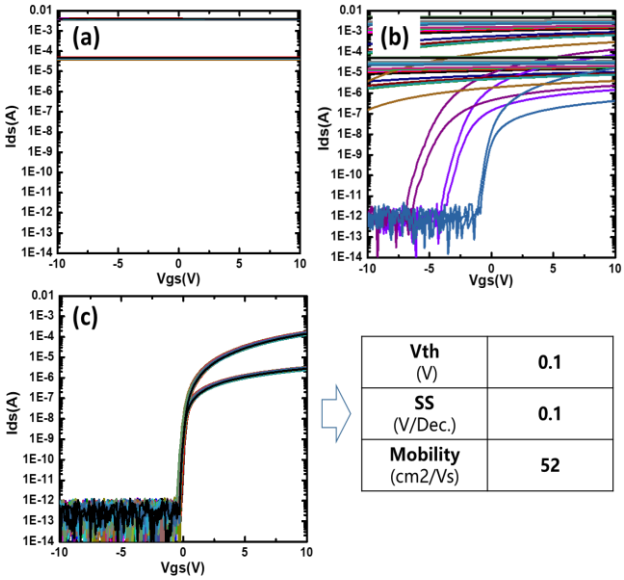
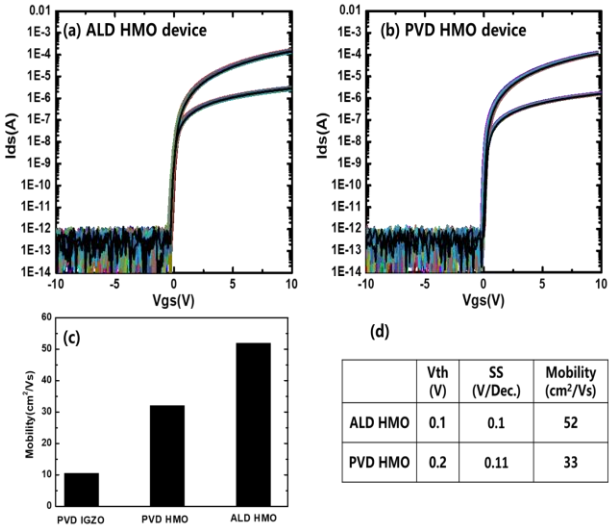


Figure 5. Id-Vg curves of high mobility oxide with different process (a) single HMO layer, (b) multi HMO layer device, (c) multi HMO layer after optimized TFT process.

Figure 5 shows ALD devices under different film layer structures and optimized TFT process conditions with a channel width and length of 4/4um. In Figure 5a, although a single-layer high-mobility oxide exhibits a high Hall mobility, but the carrier concentration is excessively high, leading to device conduction after subsequent processing. In Figure 5b, the multi-layer shows a lower carrier concentration compared to the single-layer structure. While most of the points remain conductive, some exhibit IV curves with negative shift. In Figure 5c, the multi-layer oxide after optimized TFT process, further reducing the carrier concentration, improving the uniformity in the post-processed and achieving a mobility of 52 cm²/Vs at a threshold voltage (Vth) of 0.1V. The results from Figure 3 and 5 collectively indicate that employing a stacked oxide structure combined with optimized TFT process can significantly enhances the performance and uniformity of high-mobility ALD oxide TFTs.



	Vth (V)	SS (V/Dec.)	Mobility (cm²/Vs)
ALD HMO	0.1	0.1	52
PVD HMO	0.2	0.11	33

Figure 6. IV Curves of ALD and PVD HMO device, (a) ALD HMO device, (b) PVD HMO device, (c) Mobility of different type oxide, (d) device parameter.

The improvement of mobility in oxide semiconductors is typically achieved by modifying the elemental composition of indium, gallium, and zinc in the PVD target. However, the PVD films are deposited at low temperatures, with high deposition rates, resulting in poor-quality films that contain numerous film defects, which can restrict the improvement of device mobility. In contrast, ALD thin films are deposited at high temperatures through an atomic-level layer-by-layer growth, leading to highly density films with minimal defects, which consequently obtaining higher mobility. To analyze the mobility improvement in ALD oxides, we tuned a PVD HMO device to approximate the structure and composition of the ALD HMO. The ALD and PVD high-mobility oxide devices are shown in Figure 6. The ALD oxide device has a mobility of 52cm^2/Vs at a Vth of 0.1V, whereas the PVD oxide device in Figure 6b exhibits a mobility of only 33cm^2/Vs at a comparable Vth. Under similar oxide layer, the higher mobility in ALD TFT indicates its greater potential for future AMOLED display applications.

Besides lower defect density and better film quality, ALD also allows flexible adjustment of atomic composition, enabling systematic composition optimization for further mobility enhancement. Moreover, ALD can be used to fabricate the complex multilayer structures, with individual layers thinned to atomic-scale dimensions, this can provide the additional mobility improvement through structural design.

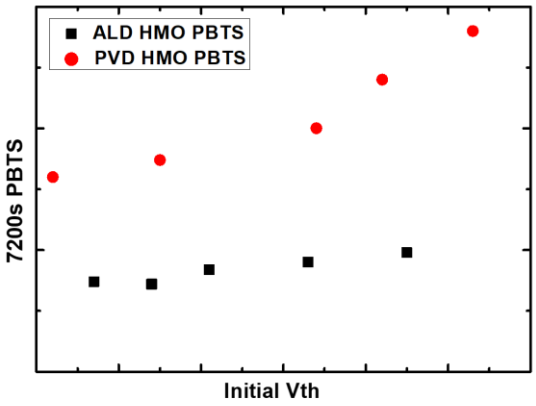


Figure 7. 7200Ss PBTS of high mobility oxide device.

Figure 7 shows the Vth shift under positive bias temperature stress (PBTS) of ALD HMO and PVD HMO. The gate bias voltage was +30V, continuously applied for 7200s at 60°C. The PBTS values of PVD HMO are larger than that of ALD HMO. Furthermore, the PBTS of PVD HMO increases significantly with higher initial Vth, whereas ALD HMO exhibits minimal dependence on the initial Vth. According to previous studies, the PBTS in oxide TFTs is primarily attributed to interface defects between the gate insulator and semiconductor layer [5]. A higher density of interface defects leads to more severe PBTS degradation. As illustrated in Figure 4, in this work, the high-mobility layer in this ALD oxide is capped by both upper and lower film layers. The ALD process offers superior film density and conformity, which helps reduce defects in the HMO layer and thus improves stress stability. Moreover, the top capping layers effectively suppress the diffusion of defects into the HMO layer, further reducing channel defects. Consequently, the ALD HMO TFT demonstrates improved PBTS stability and is less sensitive to variations in initial Vth.

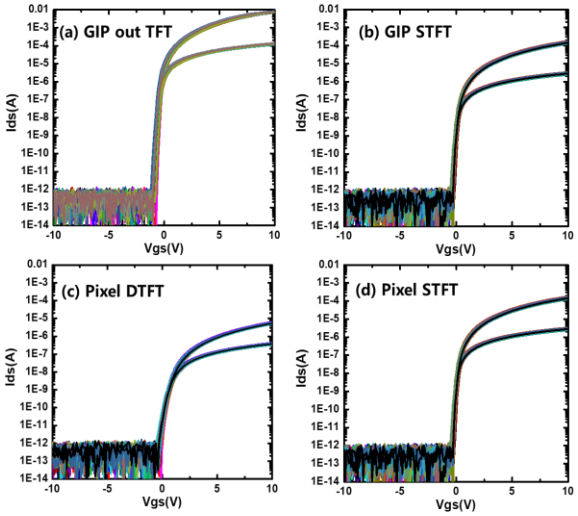


Figure 8. Device of different type TFTs of ALD high mobility oxide, (a) GIP out TFT, (b) GIP switching TFT, (c) Pixel driving TFT, (d) Pixel switching TFT.

To enable the practical application of ALD high-mobility oxides in AMOLED technology, the driving requirements of multiple functional TFTs must be satisfied, including GIP TFTs, Pixel TFTs, and ESD TFTs. Figure 8 illustrates ALD-fabricated GIP OUT, GIP Switch, Pixel Driver, and Pixel switch TFTs, where all TFT types demonstrate uniform Vth distributions on the G4.5 glass. The GIP OUT TFTs exhibit high output currents, while the Pixel Driver TFTs feature large sub-threshold swings (SS). These ALD oxide TFTs offer a high mobility of 50 $cm^2/V{\cdot}s$, a significant improvement over IGZO, leading to AMOLED panels with higher brightness and narrower bezels.

Figure 9. The AMOLED panel fabricated by ALD high mobility oxide TFT.

Figure 9 presents a 6.4 inch AMOLED panel fabricated by ALD high-mobility oxides. The panel achieves a narrow bezel, high refresh rate, and high brightness. The high-mobility oxides prepared by ALD exhibit advantages such as high mobility, low defect density, superior uniformity, and adjustable elemental composition. These properties position the ALD high-mobility oxides as a promising candidate for mass production in AMOLED display.

4. Conclusions

In this study, high-mobility oxide devices were fabricated on a G4.5 glass substrate using atomic layer deposition (ALD). Through process optimization, it was found that the low-mobility/high-mobility/low-mobility oxide stack combined with optimized TFT process can effectively reduce carrier concentration, thereby enabling the realization of high-mobility devices. The ALD high-mobility oxide devices exhibit a mobility of 52 cm^2/Vs at a Vth of 0.1 V, with a small Vth range across the G4.5 substrate. These devices simultaneously satisfy the operational requirements for both GIP circuits and pixel drivers. Consequently, a 6-inch AMOLED panel with a narrow bezel and high display brightness was successfully demonstrated, showcasing the practical potential of this ALD high-mobility oxide technology.

References

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